PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Ryoji HOSHI et al. Group Art Unit: 1722

Application No.: 10/525,244 Examiner: G.N. RAO

Filed: February 22, 2005 Docket No.: 122810

For: SINGLE CRYSTAL, SINGLE CRYSTAL WAFER, EPITAXIAL WAFER, AND METHOD OF GROWING SINGLE CRYSTAL

DECLARATION UNDER 37 C.F.R. §1.132

I, Ryoji Hoshi, a citizen of Japan, hereby declare and state:

1. I have a Master degree in Engineering which was conferred upon me by Hokkaido University in Japan in 1990.

2. I have been employed by Shin-Etsu Handotai Co., LTD since 1990 and I have had a total of 17 years of work and research experience in single silicon crystal.

3. I am a named inventor in the above-captioned patent application.

4. I have a professional relationship with the assignee of the above-identified patent application. In the course of that professional relationship, I received compensation directly from the assignee for my work relating to SINGLE CRYSTAL, SINGLE CRYSTAL WAFER, EPITAXIAL WAFER, AND METHOD OF GROWING SINGLE CRYSTAL. I am being compensated for my work in connection with this Declaration.

5. I and/or those under my direct supervision and control have conducted the following tests:

Silicon wafers cut from a grown silicon single crystal exhibit good nanotopology level when the growth rate and/or temperature fluctuation period for the crystal is controlled so that

the VxF/sinθ value is set in the range of 1.5 mm or less or 2.3 mm or more, wherein θ represents the angle to the level surface of a crystal-growth interface; V (in mm/min) represents the growth rate at the time of growing a single crystal; and F represents the temperature fluctuation period of the crystal melt. Good nanotopology level is characterized as the average of the maximum nanotopology level in the area of a 2mm x 2mm square being 14 nm or less over the whole surface of the wafer.

These properties are evidenced by the attached experimental data. In particular, experiments were carried out whereby silicon wafers were cut from a silicon single crystal grown with the VxF/sinθ value set at approximately 1.3, 2.0, and 2.6. The nanotopology was measured in a 2mm x 2mm square of each wafer. Attached Figures 1-3 depict distribution maps showing the frequency of the maximum nanotopology values as to each wafer.

Figures 1 and 3 show silicon wafers that were cut from a silicon single crystal grown with VxF/sinθ set to approximately 1.3 and approximately 2.6, respectively (i.e. values according to the presently claimed invention). Both wafers show good nanotopology level. In each wafer, the average maximum nanotopology value is 13 nm or less. Moreover, the nanotopology values over the entire surface of the wafer are highly stable and consistent. When VxF/sinθ is set to approximately 1.3, well over 90% of the wafer surface has a nanotopology level of between 12 and 13 nm. When VxF/sinθ is set to approximately 2.6, well over 90% of the wafer surface has a nanotopology level of between 11 and 13 nm. Thus, the nanotopology values are stable and highly consistent over the entire surface of the wafer. It is clear that even better nanotopology characteristics can be achieved by polishing the wafer.

In contrast, Figure 2 shows a silicon wafer that was cut from a silicon single crystal grown with VxF/sinθ set to approximately 2.0 (i.e. a conventional value outside the scope of the present claims). This wafer does not exhibit good nanotopology level. The average

maximum nanotopology value over the entire surface of the wafer is 16 nm or more. Moreover, the maximum values vary greatly over the entire surface of the wafer. It is clear that there is a limit to improvement of nanotopology characteristics when such a wafer is polished.

Accordingly, the attached data demostrates Applicants' unexpected results that silicon wafers cut from a silicon single crystal grown exhibit good nanotopology level when the growth rate and/or temperature fluctuation period for the crystal is controlled so that the VxF/sin θ value is set in the range of 1.5 mm or less or 2.3 mm or more.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and/or imprisonment under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

Date: September 10, 2007

Ryoji Hoshi